Statement of the Claims:

1. (currently amended) A method for supporting two bus masters on a single Universal Test and Operations Physical Interface for ATM (UTOPIA) ~~UTOPIA~~ bus, said method comprising:

a) coupling two bus masters to a single UTOPIA bus;

b) designating one bus master the primary bus master and the other bus master the secondary bus master;

c) coupling the secondary bus master to the primary bus master such that the secondary bus master can send a request signal to the primary bus master and the primary bus master can send a grant signal to the secondary bus master, wherein

the secondary bus master is permitted to transmit to the UTOPIA bus only after sending ~~a~~ the request signal to the primary bus master and receiving ~~a~~ the grant signal from the primary bus master.

2. (currently amended) A method according to claim 1, further comprising:

~~e~~ d) coupling the secondary bus master to the primary bus master such that the secondary bus master can send a ready signal to the primary bus master, wherein

unless the secondary bus master is malfunctioning, the primary bus master is permitted to receive from the UTOPIA bus only when the secondary bus master sends ~~a~~ the ready signal to the primary bus master.

3. (original) A method according to claim 2, wherein:

when the secondary bus master fails to send a ready signal to the primary bus master for more than one cell time, the primary bus master ignores the secondary bus master until the secondary bus master is reset.

4. (original) A method according to claim 2, wherein:

both the primary bus master and the secondary bus master receive from the UTOPIA bus at the same time.

5. (original) A method according to claim 4, wherein:

each of the primary bus master and the secondary bus master screen out received cells which belong to the other.

6. (original) A method according to claim 1, wherein:

the secondary bus master transmits to the UTOPIA bus three clock cycles after the grant signal is received.

7. (original) A method according to claim 6, wherein:

one of the three clock cycles is a dead cycle during which neither the primary bus master nor the secondary bus master controls the UTOPIA bus.

8. (original) A method according to claim 1, wherein:

the primary bus master sends a grant signal according to an arbitration scheme.

9. (original) A method according to claim 8, wherein:

the primary bus master and the secondary bus master alternate transmitting to the UTOPIA bus when both masters have cells to transmit.

10. (currently amended) A Universal Test and Operations Physical Interface for ATM (UTOPIA) ~~UTOPIA~~ bus access device, comprising:

a) a UTOPIA interface for coupling to a UTOPIA bus;

b) an Asynchronous Transfer Mode (ATM) ~~ATM~~ layer interface for coupling to an ATM layer device;

c) a control interface for coupling to another UTOPIA bus access device, said control interface including means for receiving a request signal from the other UTOPIA bus access device and means for sending a grant signal to the other UTOPIA bus access device.

11. (original) A UTOPIA bus access device according to claim 10, wherein:

said control interface includes means for receiving a ready signal from the other UTOPIA bus access device.

12. (original) A UTOPIA bus access device according to claim 10, further comprising:

d) arbitration means for determining when to send the grant signal to the other UTOPIA bus access device.

13. (original) A UTOPIA bus access device according to claim 12, wherein:

said arbitration means includes means for alternating access between said UTOPIA bus access device and the other UTOPIA bus access device when both access devices have cells to transmit.

14. (original) A UTOPIA bus access device according to claim 10, wherein:

said ATM layer interface is an interface to a repeating frame bus.

15. (currently amended) A Universal Test and Operations Physical Interface for ATM (UTOPIA) ~~UTOPIA~~ bus access device, comprising:

a) a UTOPIA interface for coupling to a UTOPIA bus;

b) an Asynchronous Transfer Mode (ATM) ~~ATM~~ layer interface for coupling to an ATM layer device;

c) a control interface for coupling to another UTOPIA bus access device, said control interface including means for sending a request signal to the other UTOPIA bus access device and means for receiving a grant signal from the other UTOPIA bus access device.

16. (original) A UTOPIA bus access device according to claim 15, wherein:

said control interface includes means for sending a ready signal to the other UTOPIA bus access device.

17. (original) A UTOPIA bus access device according to claim 15, wherein:

said ATM layer interface is an interface to a repeating frame bus.

18. (currently amended) A method for supporting two bus masters on a single Universal Test and Operations Physical Interface for ATM (UTOPIA) ~~UTOPIA~~ bus, said method comprising:

a) coupling two bus masters to a single UTOPIA bus;

b) designating one bus master the primary bus master and the other bus master the secondary bus master;

c) coupling the secondary bus master to the primary bus master such that the primary bus master controls and polls the UTOPIA bus until control is given to the secondary bus master whereupon the secondary bus master controls and polls the bus from where the primary bus master left off.

19. (currently amended) A method for supporting two bus masters on a single Universal Test and Operations Physical Interface for ATM (UTOPIA) ~~UTOPIA~~ bus to which a plurality of physical layer devices (PHYs) ~~PHYs~~ are coupled, said method comprising:

a) coupling two bus masters to a single UTOPIA bus;

b) at least one of the bus masters polling the PHYs coupled to the bus;

c) maintaining a scoreboard of all PHYs indicating which PHYs asserted the cell buffer available (CLAV) ~~CLAV~~ line in response to the most recent poll;

d) neither bus master selecting a PHY unless the scoreboard indicates that the CLAV line was asserted; and

e) resetting the scoreboard entry for a PHY when either bus master selects the PHY.